

## Dual retriggerable precision monostable multivibrator

## 74HC/HCT4538

### FEATURES

- Separate reset inputs
- Triggering from leading or trailing edge
- Output capability: standard
- I<sub>CC</sub> category: MSI
- Power-on reset on-chip

### GENERAL DESCRIPTION

The 74HC/HCT4538 are high-speed Si-gate CMOS devices and are pin compatible with "4538" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4538 are dual retriggerable-resettable monostable multivibrators. Each multivibrator has an active LOW trigger/retrigger input ( $\overline{nA_0}$ ), an active HIGH

trigger/retrigger input ( $nA_1$ ), an overriding active LOW direct reset input ( $\overline{nR_D}$ ), an output ( $nQ$ ) and its complement ( $\overline{nQ}$ ), and two pins ( $nC_{TC}$  and  $nRC_{TC}$ ) for connecting the external timing components  $C_t$  and  $R_t$ . Typical pulse width variation over temperature range is  $\pm 0.2\%$ .

The "4538" may be triggered by either the positive or the negative edges of the input pulse. The duration and accuracy of the output pulse are determined by the external timing components  $C_t$  and  $R_t$ . The output pulse width (T) is equal to  $0.7 \times R_t \times C_t$ . The linear design techniques guarantee precise control of the output pulse width.

A LOW level at  $\overline{nR_D}$  terminates the output pulse immediately.

Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{nA_0}$ , $nA_1$ to $nQ$ , $\overline{nQ}$	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	27	30	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per multivibrator	notes 1 and 2	136	138	pF

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) + 0.48 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 0.8 \times V_{CC} \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

D = duty factor in %

C<sub>EXT</sub> = timing capacitance in pF

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	OTHER
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PLH</sub>	propagation delay nA <sub>0</sub> , nA <sub>1</sub> to nQ		85 31 25	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig.8
t <sub>PHL</sub>	propagation delay nA <sub>0</sub> , nA <sub>1</sub> to nQ̄		83 30 24	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig.8
t <sub>PHL</sub>	propagation delay nR <sub>D</sub> to nQ		80 29 23	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig.8
t <sub>PLH</sub>	propagation delay nR <sub>D</sub> to nQ̄		83 30 24	265 53 45		340 68 58		400 80 68	ns	2.0 4.5 6.0	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.8
t <sub>w</sub>	nA <sub>0</sub> pulse width LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>w</sub>	nA <sub>1</sub> pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>w</sub>	nR <sub>D</sub> pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>w</sub>	nQ, nQ̄ pulse width HIGH or LOW	0.63	0.70	0.77	0.602	0.798	0.595	0.805	ms	5.0	Fig.8; R <sub>t</sub> = 10 kΩ; C <sub>t</sub> = 0.1 μF
t <sub>rem</sub>	removal time R <sub>D</sub> to nA <sub>0</sub> , nA <sub>1</sub>	35 7 6	6 2 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig.8

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		74HC								V <sub>CC</sub> (V)	OTHER
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>rt</sub>	retrigger time nĀ <sub>0</sub> , nA <sub>1</sub>	–	455+X		–		–		ns	2.0 4.5 6.0	Fig.8 X = C <sub>EXT</sub> / (4.5 × V <sub>CC</sub> )
R <sub>EXT</sub>	external timing resistor	10 2		1000 1000					kΩ	2.0 5.0	
C <sub>EXT</sub>	external timing capacitor	no limits							pF	5.0	

## NON-STANDARD DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS		
		74HC								V <sub>CC</sub> (V)	V <sub>I</sub> (V)	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
±I <sub>I</sub>	input leakage current nRC <sub>EXT</sub>			0.5		5.0		10.0	μA	6.0	2.0 or GND	V <sub>CC</sub> or GND; note 1

## Note

1. This measurement can only be carried out after a trigger pulse is applied.